Claim Amendments

This listing of the claims will replace all prior versions, and listing, of claims in the application:

Claim 1 (original): An integrated circuit (IC) chip, comprising:

a chip body having an upper side and an under side, said chip body able to be connected optionally to one of a standard wiring configuration for a standard pin assignment and to a mirror-image wiring configuration for a mirror-image pin assignment, the mirror-image wiring configuration being mirror-inverted in relationship to the standard wiring configuration; and

at least two groups of metallic bonding pads disposed on one of said upper side and said under side of said chip body, a first group of said at least two groups of said metallic bonding pads ordered in the standard pin assignment, a second group of said at least two groups of said metallic bonding pads ordered in the mirror-image pin assignment.

Claim 2 (currently-amended): The IC chip according to claim 1, wherein given the standard wiring configuration for the

standard pin assignment and the mirror-image wiring configuration for the mirror-image pin assignment, the standard pin ~~alignment~~ assignment is realized by a positioning of said chip body in a first position, the mirror-image pin assignment realized by a positioning of said chip body in a second position and once in the second position can be transformed into the first position by rotation of said chip body about an axis aligned perpendicularly in relation to said upper side or said underside of said chip body or by a translational movement of said chip body along a straight line, running parallel to said upper side or to said underside of said chip body.

Claim 3 (original): The IC chip according to claim 2, wherein for a transformation from the second position into the first position, and vice versa, in each case, rotating said IC chip body by one of 90°, 180° and 270° is required.

Claim 4 (original): The IC chip according to claim 2, wherein said standard wiring configuration and said mirror-image wiring configuration in each case extends on two opposite sides of said chip body over said chip body.

Claim 5 (original): The IC chip according to claim 2, wherein said first group of said metallic bonding pads is disposed in

a first row and said second group of said metallic bonding pads is disposed in a second row on said chip body.

Claim 6 (original): The IC chip according to claim 5, wherein said first row and said second row are disposed next to each other.

Claim 7 (original): The IC chip according to claim 5, wherein said metallic bonding pads of said first row and said metallic bonding pads of said second row have within their own row, in each case, a same spacing in relation to directly neighboring bonding pads.

Claim 8 (original): The IC chip according to claim 5, wherein said metallic bonding pads of said first row and said metallic bonding pads of said second row each lie along one of two straight lines running parallel to each other.

Claim 9 (original): The IC chip according to claim 8, wherein said metallic bonding pads in said first row and said metallic bonding pads in said second row lie directly opposite one another and in each case lie along a further straight line, running perpendicularly in relation to the two straight lines.

Claim 10 (original): The IC chip according to claim 5, wherein pins of said standard pin assignment of said metallic bonding pads of said first group along said first row are assigned in a same direction as pins of the mirror-image pin assignment of said metallic bonding pads of said second group.

Claim 11 (original): The IC chip according to claim 5, wherein for a transformation from the second position of said chip body into the first position, and vice versa, in each case a translational movement transversely in relation to said first and second rows is required.

Claim 12 (original): The IC chip according to claim 1, wherein said metallic bonding pads of said first group and of said second group are disposed in an alternating manner in a common row.

Claim 13 (original): The IC chip according to claim 12, wherein said metallic bonding pads of said first group and of said second group in said common row have in each case a same spacing in relation to directly neighboring bonding pads of the other group respectively.

Claim 14 (original): The IC chip according to claim 12, wherein pins of said standard pin assignment of said metallic

bonding pads of said first group and pins of said mirror-image pin assignment of said metallic bonding pads of said second group both lying along said common row are assigned in a same direction.

Claim 15 (original): The IC chip according to claim 5, wherein pins of said standard pin assignment of said metallic bonding pads of said first group along said first row are assigned in an opposite direction than pins of said mirror-image pin assignment of said metallic bonding pads of said second group.

Claim 16 (original): The IC chip according to claim 12, wherein for a transformation from the second position of said chip body to the first position, and vice versa, in each case a translational movement along said common row is required.

Claim 17 (original): The IC chip according to claim 12, wherein said metallic bonding pads of said first group and of said second group lying in said common row lie along a straight line.

Claim 18 (original): A component placement method, which comprises the steps of:

providing an integrated circuit chip containing a chip body having an upper side and an under side, the chip body able to be connected optionally to one of a standard wiring configuration for a standard pin assignment and to a mirror-image wiring configuration for a mirror-image pin assignment, the mirror-image wiring configuration being mirror-inverted in relationship to the standard wiring configuration, at least two groups of metallic bonding pads disposed on one of the upper side and the under side of the chip body, a first group of the at least two groups of the metallic bonding pads ordered in the standard pin assignment, a second group of the at least two groups of the metallic bonding pads ordered in the mirror-image pin assignment; and

using the integrated circuit for placing components on at least one side of a printed circuit board using surface mounting techniques.